## REMARKS

The Office Action dated June 24, 2005, has been received and carefully noted. The following remarks, are submitted as a full and complete response thereto. Claims 1-60 are presently pending in the subject application and are respectfully submitted for consideration.

Claims 1-60 were rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over U.S. Patent No. 6,021,132 (Muller et al.) in view of U.S. Patent No. 6,529,519 (Steiner et al.), and further in view of U.S. Patent No. 5,860,136 (Fenner). The Office Action took the position that Muller and Steiner taught all the elements of the claims 1-60, with the exception of an index key. Fenner was cited as providing the elements missing from Muller and Steiner. Applicants respectfully submit that Muller, Steiner and Fenner, either alone or in combination, fail to disclose or suggest all the features of any of the presently pending claims.

Claim 1, upon which claims 2-7 are dependent, recites a memory structure. The memory structure includes an Address Resolution Table for resolving addresses in a packet-based network switch and using a key to index a location within the Address Resolution Table. The memory structure also includes a Packet Storage Table, the Packet Storage Table adapted to receive a packet for storage in the packet-based network switch, and sharing a preselected portion of memory with the Address Resolution Table. The memory structure also includes a single buffer per packet mechanism configured to

receive an individual packet for enabling only one transmit descriptor read per the individual packet and for enabling an execution of a single access in order to locate an entire packet at the location using the key. The entire packet is to be transmitted.

Claim 8, upon which claims 9-12 are dependent, recites a memory structure. The memory structure includes an Address Resolution Table having an associative memory structure and using a key to index a location within the Address Resolution Table. The Address Resolution Table resolves addresses in a packet-based network switch. The memory structure also includes a single buffer per packet mechanism configured to receive an individual packet for enabling only one transmit descriptor read per the individual packet and for enabling an execution of a single access in order to locate an entire packet at the location using the key. The entire packet is to be transmitted.

Claim 13, upon which claims 14-27 are dependent, recites a memory structure having a memory block. The memory structure includes an Address Resolution Table having an associative memory structure. The Address Resolution Table resolves addresses in a packet-based network switch and using a key to index a location within the Address Resolution Table. The memory structure also includes a Transmit Descriptor Table. The Transmit Descriptor Table is associated with a corresponding packet-based network transmit port, and the Transmit Descriptor Table is adapted to receive a Table Descriptor Address and a Table Descriptor Value. The memory structure also includes a Packet Storage Table. The Packet Storage Table is adapted to receive at least one of each of a Packet Data Address portion and a Packet Data Value portion. The memory

structure also includes a single buffer per packet mechanism configured to receive an individual packet for enabling only one transmit descriptor read per the individual packet and for enabling an execution of a single access in order to locate an entire packet at the location using the key. The entire packet is to be transmitted.

Claim 28, upon which claims 29-31 are dependent, recites a packet-based switch. The packet-based switch includes a shared memory structure having an Address Resolution Table and a Packet Storage Table. The packet-based switch also includes a key to index a location within the Address Resolution Table. The packet-based switch also includes a single buffer per packet mechanism configured to receive an individual packet for enabling only one transmit descriptor read per the individual packet and for enabling an execution of a single access in order to locate an entire packet at the location using the key. The entire packet is to be transmitted.

Claim 32, upon which claims 33-51 are dependent, includes some of the features of claim 13, but is drawn to a packet-based switch.

Claim 52, upon which claims 53-56 are dependent, includes some of the features of claim 8, but is drawn to a packet-based switch.

Claim 57, upon which claims 58-60 are dependent, includes some of the features of claim 8, but is drawn to a packet-based switch.

As discussed in the specification, examples of the present invention enable a memory structure to resolve addresses in a packet-based network switch. Examples of the present invention enable bandwidth savings that are attributed to a one buffer-per-

packet approach. The single buffer-per-packet approach enhances the feasibility of a bit-per-buffer pool tracking technique and the need to search a larger buffer structure can be mitigated or eliminated. Thus, a packet-based switch performs one memory read for address resolution, and one memory write for address learning, to the address table for each frame received. Overhead is reduced and a reduction in accesses per frame is achieved. The single access for both read and write can be attributed to the single-entry direct-mapped address table. Applicant respectfully submits that the cited references of Muller, Steiner and Fenner, when viewed alone or combined, fail to disclose or suggest all the elements of the presently pending claims. Therefore, the cited references fail to provide the critical and unobvious advantages discussed above.

Muller relates to shared memory management in a switch network element. Muller describes a shared memory manager 220 that is exploited by input and output ports 206 by locally storing pointers to buffers that contain packet data rather than locally storing the packet data. A predetermined number of buffer pointers are kept on hand to allow immediate storage of received packet data. The buffer pointers are preallocated during the initialization of switching element 100 and requested from shared memory manager 220. Pointers are queued to buffers that contain packet data, and not to the packet data itself. Further, a packet can be stored over more than one buffer. Each buffer in shared memory 230 is owned by one or more different ports at different points in time without having to duplicate the packet data.

Steiner relates to prioritized-buffer management for fixed size packets in a multimedia application. Steiner describes a memory system that includes a tag register for storing tags associated with respective pages, wherein each tag indicates whether the associated page is empty or full. Steiner also describes a shadow register for storing conflict-free updates from the tag register and a page register for storing pointers to the lowest free or unoccupied page. Steiner also describes a buffer that is organized along packet boundaries or pages for convenience of operation. A processor maintains a table of pointers to each packet boundary, and, therefore, knows the location of all leftover packets. A tag register 40 is provided, that has as many bits as there are packet boundaries of buffer 22.

Fenner relates to a method and apparatus for use of associated memory with large key spaces. Fenner describes an associative memory that utilizes a location addressable memory and a lookup table to generate, from a key, the address in memory storing an associated record. Fenner describes an associative memory utilizing arithmetic coding to associate a key presented to the memory with a record stored in the memory. The associative memory includes an index table stored in memory and a record memory for storing the records of data. The index table is constructed so that each symbol of a key, with a key being divided into a string of symbols and each symbol being defined by its position within the key and its value, addresses an index value in the index table memory. The index values are assigned such that the sum of index values for a given key is a unique value that is used to address the record memory.

Applicants submit that the cited references of Muller, Steiner and Fenner, either alone or in combination, fail to disclose or suggest all the features of any of the presently pending claims. For example, the cited references fail to disclose or suggest enabling an execution of a single access in order to locate an entire packet at a location using a key, wherein the entire packet is to be transmitted. As discussed in previous responses, Muller and Steiner fail to disclose or suggest at least this feature of the claims. Referring to Muller, pointers are allocated to buffers as packets are received at the input port. As noted above, the buffers are kept on hand to allow storage of received data packets. The pointers of Muller, however, fail to use a key to index a location in the Address Resolution Table. Further, Muller describes a data packet being stored in more than one buffer. Muller fails to enable an execution of a single access in order to locate an entire packet at the location using the key. Applicants submit that Muller does not disclose or suggest locating an entire packet using a key, but uses the stored pointers to piece together a packet which may be stored over several buffers. Thus, Muller does not disclose or suggest at least these features of the pending claims.

Applicants also submit that Steiner, either alone or in combination with Muller, fails to disclose or suggest the features of the claims missing from Muller. Steiner describes using pointers and a tag register to each packet boundary within a buffer, also known as "pages." Steiner, however, fails to disclose or suggest using a key to index a location within the buffer, or to a page within the buffer. Instead, Steiner uses a processor to maintain a table of pointers and the tag register. The processor fails to use a

key to index the table of pointers or the tag register. Further, the processor reads the contents of a shadow register to determine how many packets are in a buffer. Thus, Steiner fails to disclose or suggest a single buffer per packet mechanism for enabling an execution of a single access in to locate an entire packet at the location using the key.

Applicants submit that Fenner, either alone or in combination with Muller and Steiner, fail to disclose or suggest the features of the claims missing from Muller and Steiner. Fenner describes using arithmetic coding to associate a key presented to a memory with a record stored in the memory. Fenner fails to enable a single access in order to locate an entire packet at a location using a key, wherein the entire packet is to be transmitted. Fenner, instead, uses index values assigned such that the sum of the index values for a key is a value that is used to address the record memory. Fenner fails to execute a single access to locate an entire packet to be transmitted from a network switch. For at least these reasons, Fenner fails to disclose or suggest the features of the claims missing from Muller and Steiner.

Applicants also submit that no evidence is provided of a motivation or suggestion to combine the references, either in the references themselves or in the knowledge generally available to one skilled in the art. Applicants note that Fenner is cited by the Office Action because it teaches an index key. The Office Action does not provide any evidence to combine the index key with Muller and Steiner to achieve applicants' claimed invention. Applicants note that a piecemeal analysis of a number of references, to extract a number of individual elements that are picked and chosen to recreate the

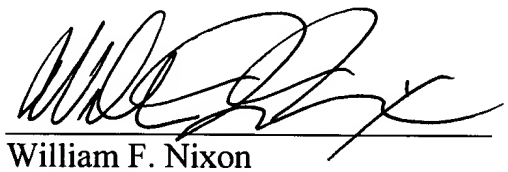
claimed invention, is improper absent some teaching or suggestion in the references to support their use in the particular claimed combination. "Before the PTO may combine the disclosures of two or more prior art references in order to establish *prima facie* obviousness, there must be some suggestion for doing so, found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art." In re Jones, 21 USPQ2d 1941, 1943-44 (Fed. Cir. 1992). Thus, applicants maintain that the obviousness rejection of claims 1-60 is improper for at least the reasons give above. Applicants respectfully request that the obviousness rejection be withdrawn.

Applicants further submit that each of claims 1-60 recites subject matter that is neither disclosed nor suggested by the cited references. It is therefore respectfully requested that all of claims 1-60 be allowed, and this application passed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the applicants respectfully petition for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,



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